

1       **ABSTRACT OF THE DISCLOSURE**

2       **Apparatus and methods implemented in a processor semiconductor logic chip for providing**  
3       **novel "hint instructions" that uniquely preserve and reuse branch predictions replaced in a**  
4       **branch history table (BHT). A branch prediction is lost in the BHT after its associated**  
5       **instruction is replaced in an instruction cache. The unique "hint instructions" are**  
6       **generated and stored in a unique instruction cache which associates each hint instruction**  
7       **with a line of instructions. The hint instructions contains the latest branch history for all**  
8       **branch instructions executed in an associated line of instructions, and they are stored in the**  
9       **instruction cache during instruction cache hits in the associated line. During an instruction**  
10       **cache miss in an instruction line, the associated hint instruction is stored in a second level**  
11       **cache with a copy of the associated instruction line being replaced in the instruction cache.**  
12       **In the second level cache, the copy of the line is located through the instruction cache**  
13       **directory entry associated with the line being replaced in the instruction cache. Later, the**  
14       **hint instruction can be retrieved into the instruction cache when its associated instruction**  
15       **line is fetched from the second level cache, and then its associated hint instruction is also**  
16       **retrieved and used to restore the latest branch predictions for that instruction line. In the**  
17       **prior art this branch prediction would have been lost. It is estimated that this invention**  
18       **improves program performance for each replaced branch prediction by about 80%, due to**  
19       **increasing the probability of BHT bits correctly predicting the branch paths in the**  
20       **program from about 50% to over 90%. Each incorrect BHT branch prediction may result**  
21       **in the loss of many execution cycles, resulting in additional instruction re-execution**  
22       **overhead when incorrect branch paths are belatedly discovered.**